REMARKS

Claims 1-25 are pending. Claim 24 is being amended. No new matter is presented.

Claims 1-3 and 23 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,453,281 to Walters et al. ("Walters") in view of U.S. Patent No. 5,491,774 to Norris et al. ("Norris").

An embodiment of the present invention provides an electronic device for the recording/reproduction of voice data that is entirely integrated in a chip of semiconductor material. It should be emphasized that the components of the electronic device, including the main transmission line, control unit, signal-conversion unit and non-volatile memory unit, are *all integrated in the same chip*. The advantages of this single-chip integration include a smaller device size and reduced power consumption. In addition, the unique architecture of the single-chip integration enables the device to optimize editing of the voice messages itself. Furthermore, the embodiment is characterized by the ability to accept and emit audio signals according to different formats by virtue of an interface circuit. This interface circuit adapts the format of data exchanged between the signal-conversion unit and the memory unit and implements a strategy of recovery of commands lost or failed.

Walters and Norris do not teach or such the invention recited in claim 1. Claim 1 recites "An electronic device for the recording/reproduction of voice data, comprising: a chip of semiconductor material; a main transmission line *integrated in said chip*; a control unit *integrated in said chip*...; a signal-conversion unit *integrated in said chip*; and a non-volatile memory unit *integrated in said chip*..." (Emphasis added.) As admitted by the Examiner, Walters does not teach the integration in a single chip of such control, signal-conversion, and memory units.

Norris also does not suggest integrating such control, signal-conversion, and memory units in a single chip. Norris discloses control circuitry 21 coupled to a non-volatile flash memory module 29 by an electronic interconnect 28 (Figure 1). Norris explicitly states that the flash memory module 29 is removable (see col. 3, lines 50-64), and further states that it is comprised of three separate chips 80-82 and other circuit elements shown in Figures 6A and 6B (col. 9, lines 46-57). Accordingly, Norris would not have taught one skilled in the art to

integrate a non-volatile memory module on the same chip as a main transmission line, control unit, and signal conversion unit.

The Examiner points to an item 37 of Figure 1 of Norris as an integrated circuit, but the Examiner is mistaken. Item 37 is shown in Figure 3, rather than Figure 1, and is a record control button (col. 4, lines 50-58).

In Figure 1, Norris shows the control circuitry 21 as including several parts 22-26, but that does not suggest integrating a non-volatile memory unit in the same chip as a main transmission line, control unit, and signal conversion unit. In particular, Norris never suggests that the control circuitry 21 can or should be implemented as an integrated circuit on a single chip. Instead, Norris states that Figure 1 is functional block diagram rather a physical layout (col. 3, lines 32-33; col. 5, lines 46-48). In addition, Figure 2, which provides additional detail of the function diagram of Figure 1 (col. 3, lines 34-35), shows the signal processing circuitry 22 and playback circuit 25 as separate modules from a microprocessor 21. Moreover, Norris also states that a separate CODEC 42 performs the A/D conversion that is shown in Figure 1 as A/D conversion circuitry 23 of the control circuitry 21.

Even if the control circuitry 21 were implemented as an integrated circuit on a single chip, Norris still would not teach integrating a non-volatile memory unit in the same chip as a main transmission line, control unit, and signal conversion unit. Norris shows memory circuitry 24 as part of the control circuitry 21, but Norris never suggests that the memory circuitry 24 is a non-volatile memory unit or even a memory unit that stores data. Instead, the discussion of the operation of the Norris system implies that the memory circuitry 24 functions as memory control circuitry for storing data in the detachable flash memory module 29 (col. 4, lines14-18; col. 6, lines 5-39). Thus, the memory circuitry 24 is not a non-volatile memory unit integrated with a control unit.

For the foregoing reasons, claim 1 is nonobvious in view of the cited prior art.

Claims 2-3 and 23 depend on claim 1, and thus, also nonobvious.

In addition, claim 23 recites other features that are not taught or suggested by Walters and Norris. In particular, claim 23 recites that the non-volatile memory unit includes a format adapter for adapting the format of the first stream of compressed digital signal for the

non-volatile memory unit. Neither Walters nor Norris mentions or suggests such a format adapter. That fact, by itself, is enough to make claim 23 nonobvious in view of the prior art.

The applicants disagree for several reasons with the Examiner's assertion that "it was obvious that the memory unit 122 contained a format adapter since CODEC encoded the incoming voice signals according to a unique compression algorithm and the memory was adapted to store the voice signals according to that compression algorithm." First, an unsupported conclusion that the memory unit contained a format adapter does not satisfy the Examiner's burden of showing a specific teaching in the prior art of each claim element. In re Glaug, 283 F.3d 1335, 1341-1342 (Fed. Cir. 2002) (copy attached). Second, nothing in the function or structure of Walter's system inherently requires the memory unit 122 to include a format adapter. The output of the CODEC 158 could be in a format that is already compatible with the memory unit 122, and thus, there would be no need for the memory unit 122 to include a format adapter. Third, even if the Examiner were correct that the memory unit 122 was adapted to store the voice signals from the CODEC, that does not mean that the memory unit 122 necessarily includes a format adapter. Instead, the underlying structure of the memory unit could be redesigned to be compatible with the voice signals from the CODEC without needing a particular format adapter.

Thus, claim 23 is in condition for allowance.

Claims 4-5, 12-13, and 15-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters and Norris in view of Unno et al., EP 0 851 423 A1 ("Unno").

Walters, Norris and Unno do not teach or suggest the invention recited in claims 4 and 5, which depend on claim 1. Unno does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters and Norris do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Unno (a buffer memory) would not satisfy the limitations of claims 4 and 5. Accordingly, claims 4-5 are nonobvious in view of the cited prior art.

Although the language of claims 12-13 and 15-16 is not identical to that of claims 4-5, the nonobviousness of claims 12-13 and 15-16 will be apparent in view of the above discussion.

Although the language of claims 24 and 25 is not identical to that of claim 23, the nonobviousness of claims 24-25 will be apparent in view of the above discussion.[1]

Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters, Norris, and Unno in view of U.S. Patent No. 5,787,445 to Daberko.

The cited prior art references do not teach or suggest the invention recited in claims 6 and 7, which depend from claim 1. Daberko does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters, Norris, and Unno do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Daberko (first and second cache memories) would not satisfy the limitations of claims 6 and 7. Accordingly, claims 6-7 are nonobvious in view of the cited prior art.

Claims 8, 14, and 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters, Norris, and Unno in view of U.S. Patent No. 6,016,522 to Rossum.

The cited prior art references do not teach or suggest the invention recited in claim 8, which depends from claim 1. Rossum does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters, Single, and Unno do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Rossum ("ping-pong" buffering) would not satisfy the limitations of claim 8. Accordingly, claim 8 is nonobvious in view of the cited prior art.

Although the language of claims 14 and 17-19 is not identical to that of claim 8, the nonobviousness of claims 14 and 17-19 will be apparent in view of the above discussion.

Claims 9-11 and 20-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters and Norris in view of U.S. Patent No. 6,604,168 to Ogawa.

Walters, Norris, and Ogawa do not teach or suggest the invention recited in claims 9-11. Ogawa does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters and Norris do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of

[1] The Examiner failed to address claims 24-25, which were added in the amendment filed December 16, 2004. However, given the similarity of claims 24-25 to claim 23, the applicants are treating claims 24-25 as if they were rejected.

Ogawa would not satisfy the limitations of claims 9-11. Accordingly, claims 9-11 are nonobvious in view of the cited prior art.

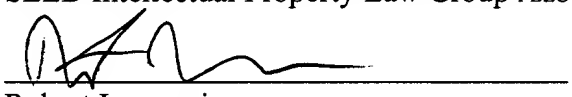
Although the language of claims 20-22 is not identical to that of claims 9-11, the nonobviousness of claims 20-22 will be apparent in view of the above discussion.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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